ABSTRACT OF THE DISCLOSURE

A method and system for accelerating software simulator operation with the aid of reprogrammable hardware such as Field Programmable Gate Array devices (FPGA). The method and system aid in emulation and prototyping of Application Specific Integrated Circuits (ASIC) digital circuit designs by means of reprogrammable devices. The system includes a design verification manager and software program that includes subroutines of finding clock sources, finding synchronous primitives that are receiving clock signals from the clock sources, and a subroutine for inserting edge detector circuits between such clock sources and synchronous primitives. This new method allows eliminating of clock timing issues by applying basic design clocks to the clock enable instead of clock trigger inputs and generating and applying to clock trigger inputs a new clock that is automatically delayed in respect to all other clocks in the design. This system solves the major obstacle for automatic retargeting of ASIC designs into reprogrammable devices that have different timings of the clocking chains in ASICs and FPGAs that result in triggering of associated flip-flops and latches at different times.